

ABSTRACT

PN - JP2003282465 A 20031003
 TI - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
 AB - <P>PROBLEM TO BE SOLVED: To increase the plasma decomposition efficiency of a PFC gas.
 <P>SOLUTION: In a wafer treatment chamber 41 of semiconductor manufacturing equipment 40 built into a CVD apparatus 40a, a film formation process is conducted on a wafer W2 by a CVD method. After film formation is finished, a PFC gas is supplied as cleaning gas into the wafer treatment chamber 41. An unconsumed portion of the PFC gas which has not been used for cleaning the inside of the wafer treatment chamber 41 is sent out to a plasma decomposition chamber 21 of a PFC gas removing apparatus 20. The prescribed quantity of an inert gas such as nitrogen is supplied into the plasma decomposition chamber 21 together with additional gases such as an oxygen and water steam, and the PFC gas is subjected to plasma decomposition under the presence of the inert gas. <P>COPYRIGHT: (C)2004,JPO
 FI - B01D53/34&134E; B01J19/08&E; C23C16/44&J; H01L21/205+ZAB; H01L21/302&101H; H05H1/46&M
 PA - HITACHI LTD; RENASAS NORTHERN JAPAN SEMICON
 IN - KUBOTA TETSUYA
 AP - JP20020086464 20020326
 PR - JP20020086464 20020326
 DT - I

CLAIMS

AN - 2003-885126 [82]
 TI - Manufacture of semiconductor device e.g. MISFET, involves plasma decomposition of perfluoro compound gas in presence of gas containing inert gas
 AB - JP2003282465 NOVELTY - The manufacturing of semiconductor device involves plasma decomposition of perfluoro compound (PFC) gas in the presence of a gas containing inert gas.
 - USE - For manufacturing semiconductor device, e.g. MISFET, EEPROM.
 - ADVANTAGE - The manufacturing method provides improved plasma decomposition efficiency of PFC gas, and is eco-friendly.
 - DESCRIPTION OF DRAWING(S) - The figure shows the explanatory drawing of the semiconductor manufacturing apparatus used for the manufacture of semiconductor device. (Drawing includes non-English language text).
 - plasma decomposition chamber 21
 - electrode 22
 - high-frequency electric power unit 23
 - semiconductor manufacturing apparatus 40
 - chemical vapor deposition apparatus 40a
 - (Dwg.2/8)
 IW - MANUFACTURE SEMICONDUCTOR DEVICE MISFET PLASMA DECOMPOSE COMPOUND GAS PRESENCE GAS CONTAIN INERT GAS
 PN - JP2003282465 A 20031003 DW200382 H01L21/205 012pp
 IC - B01D53/70 ; B01J19/08 ; C23C16/44 ; H01L21/205 ; H01L21/3065 ; H05H1/46
 MC - L04-X
 - U11-C15Q V05-F05C V05-F05E5 V05-F08X X14-F
 DC - L03 U11 V05 X14
 PA - (HITW) HITACHI HOKKAI SEMICONDUCTOR
 - (HITA) HITACHI LTD
 AP - JP20020086464 20020326
 PR - JP20020086464 20020326

EFFECT

PN - JP2003282465 A 20031003
 TI - METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
 AB - PROBLEM TO BE SOLVED: To increase the plasma decomposition efficiency of a PFC gas.

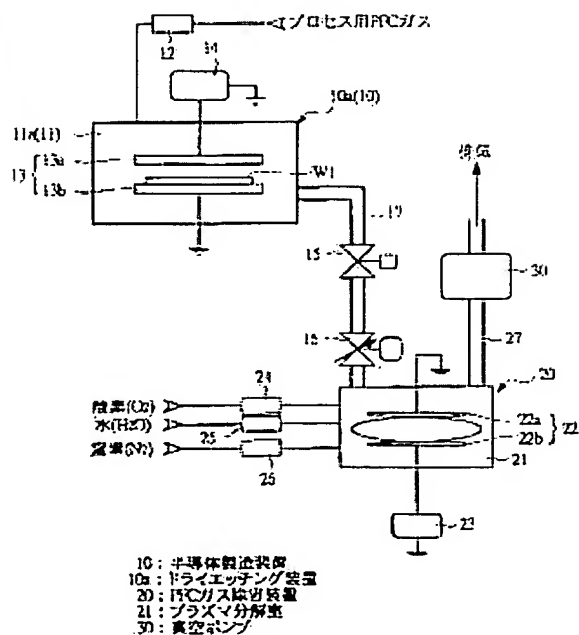
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I - H01L21/205 ; B01D53/70 ; B01J19/08 ; C23C16/44 ; H01L21/3065 ; H05H1/46
IPA - HITACHI LTD; RENASAS NORTHERN JAPAN SEMICONDUCTOR INC
IN - KUBOTA TETSUYA
ABD - 20031205
ABV - 200312
AP - JP20020086464 20020326

- 13a 電極
- 13b 電極
- 14 高周波電源
- 15 電磁弁
- 16 圧力調整弁
- 17 配管
- 20 PFCガス除去装置
- 21 プラズマ分解室
- 22 電極
- 22a 電極
- 22b 電極
- 23 高周波電源
- 24 流量制御装置
- 25 流量制御装置
- 26 流量制御装置
- 27 配管
- 30 真空ポンプ
- 40 半導体製造装置
- 40a CVD装置
- 41 ウェハ処理室
- 41a CVDチャンバ
- 42 サセプタ
- 43 シャワープレート
- 44 流量制御装置

〔図1〕

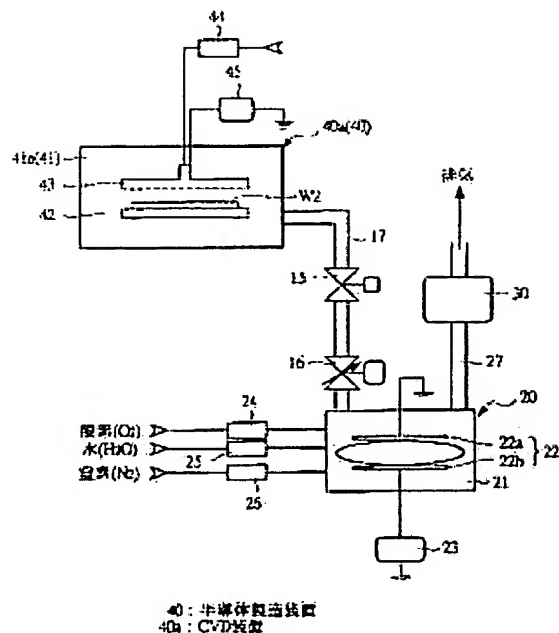
図 1



- * 45 高周波電源
- 111 n⁺型半導体領域
- 112 n⁺型半導体領域
- 113 p⁺型半導体領域
- 114 p⁺型半導体領域
- 115 酸化シリコン膜
- 116 素子分離
- 117 p型ウェル
- 118 n型ウェル
- 119 ゲート酸化膜
- 121 多結晶シリコン膜
- 122 窒化シリコン膜
- 123 サイドウォールスペーサ
- 124 酸化シリコン膜 (TEOS膜)
- 125 コンタクトホール
- 126 コンタクトホール
- 127 ブラダ
- 130 第1層配線
- 131 第1層配線
- 132 第1層配線
- 133 第1層配線
- G ゲート電極
- W1 ウェハ
- W2 ウェハ

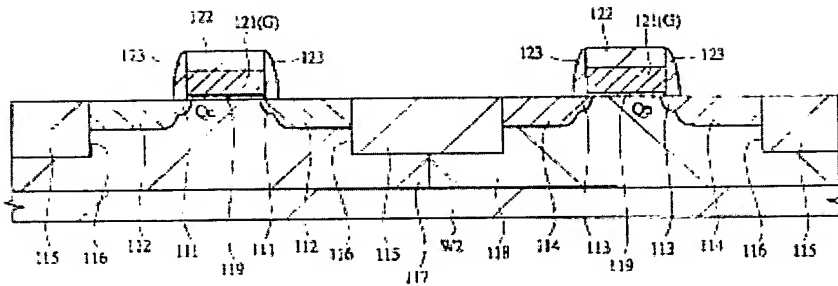
〔図2〕

図 2



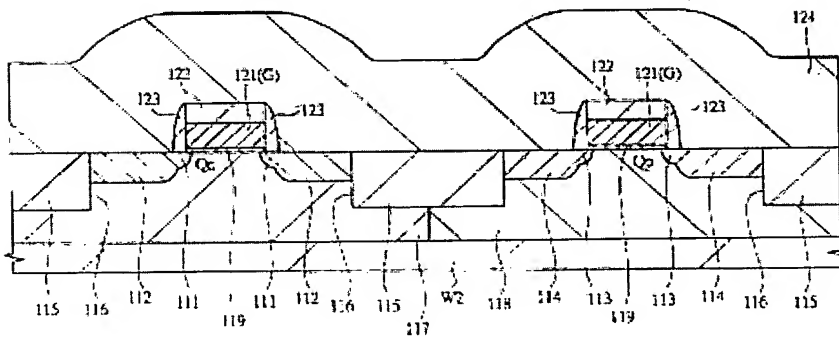
【図3】

図 3



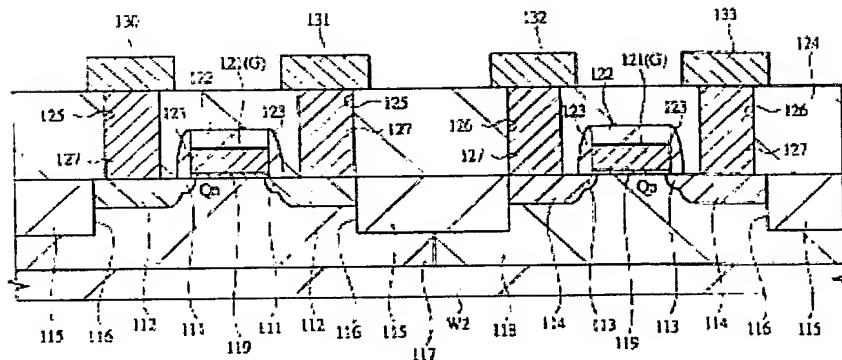
【図4】

図 4



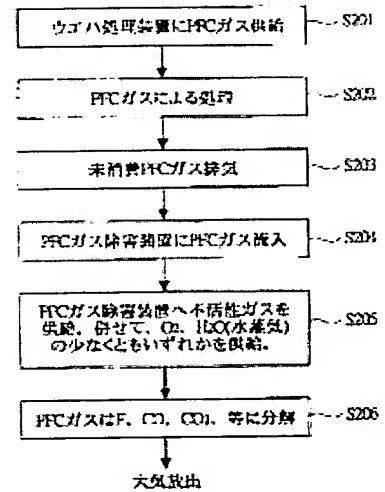
【図5】

図 6



【図5】

図 5

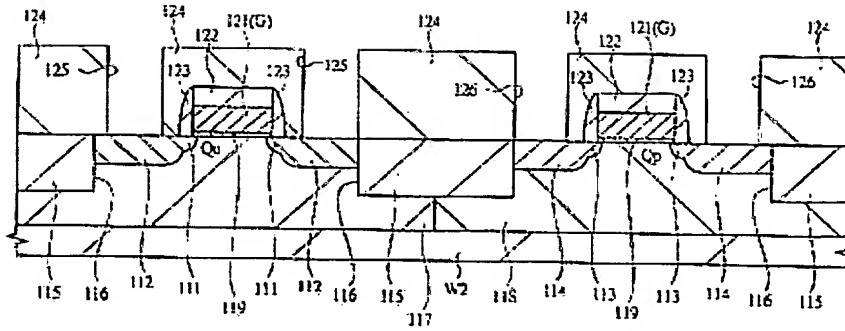


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(51)Int
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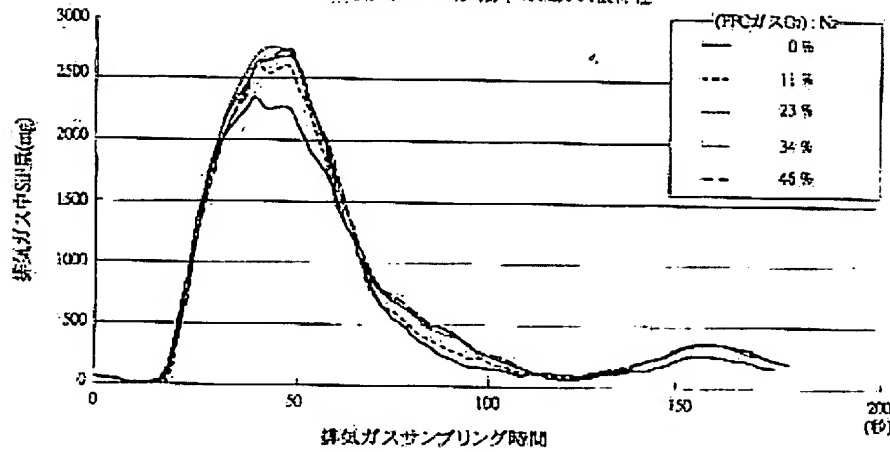
(図7)

図 7



(図8)

図 8

SiO₂膜クリーニング効率のN₂ガス依存性

フロントページの続き

(52)Int.Cl.

H05H 1/46

識別記号

F1

B01D 53/34

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134E

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